7. (Amended) A semiconductor device according to claim 5, wherein the gate insulating film is a tunnel gate insulating film, and ~~the gate electrode~~ is a floating gate electrode.

REMARKS

In this Amendment, Applicants have canceled claim 6 without prejudice or disclaimer of the subject matter therein, and amended claims 1 – 5 and 7 to more appropriately define the invention. Applicants submit that the amendments to claims 1 – 5 and 7 do not diminish or limit their scope. In accordance with the requirements of 37 C.F.R. § 1.121(c)(1), Applicants provide a marked-up version of the amended claims in an attached Appendix designated "Version of Claims with Markings to Show Changes Made." Claims 1 – 5 and 7 remain pending.

In the October 10, 2001 Office Action, the Examiner acknowledged items listed on Applicants' Information Disclosure Statement; rejected claims 1 – 4 under 35 U.S.C. § 103(a) as unpatentable over Rhee (U.S. Patent No. 5,646,054) in view of Teramoto (U.S. Patent No. 5,620,910); rejected claims 5 and 6 under 35 U.S.C. § 103(a) as unpatentable over Rhee and Teramoto as applied to claim 1 and further in view of Takemura (U.S. Patent No. 5,917,221); and rejected claim 7 under 35 U.S.C. § 103(a) as unpatentable over Rhee, Teramoto, and Takemura as applied to claim 5 and further in view of Tomita et al. (U.S. Patent No. 5,959,329).

Regarding the claims, Applicants respectfully traverse the rejection of claims 1 – 7, as detailed above, for the following reasons.

Regarding the 35 U.S.C. § 103(a) rejection of claims 1 – 4, Applicants respectfully disagree with the Examiner's arguments and conclusions. The Examiner: (1) does not show that all the elements of Applicants' claims are met in the cited references, taken alone or in combination; (2) does not show that there is any suggestion or motivation to modify the applied

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references to result in the claimed invention; and (3) does not show that there is a reasonable expectation of success from modifying the applied references.

Applicants' claim 1 recites, *inter alia*, "a semiconductor substrate having a main plane in which a channel of a transistor is formed, the semiconductor substrate comprising a first region and a second region defined in a section taken along a direction of a channel length, the second region having a surface located lower than that of the first region, and the second region being connected to the first region."

Applicants refer the Examiner to Rhee's Figure 7, specifically the central region around gate electrodes 62 and 64, which is a cross-sectional view of high breakdown voltage MOS transistors (Rhee, column 7, lines 7 – 8). This cross-section is taken in the direction of the channel width. A p-type semiconductor substrate 40 and P-well 42 are shown with a flat area between low-concentration impurity layers 55 on the left and right. Rhee does not disclose anything about the structure, layout, or regions of semiconductor substrate 40, P-well 42, gate insulating film 60, or poly-Si gate electrodes 62 and 64, in a section taken along a direction of a channel length (when viewing Rhee's Figure 7, the channel length cross-sectional view would be in the direction perpendicular to the paper). As such, Rhee does not disclose a first or second region on semiconductor substrate 40 or P-well 42 "defined in a section taken along a direction of a channel length, the second region having a surface located lower than that of the first region, and the second region being connected to the first region," which is recited, *inter alia*, in Applicants' claim 1. One can only discern one region on P-well 42 taken in the direction of the channel width, and not any information in the direction of the channel length.

For illustrative purposes only, Applicants refer the Examiner to Figure 2A showing an embodiment of the present invention, which depicts, in contrast, an exemplary cross-sectional

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view taken along the channel length. Substrate 1 is clearly shown with two regions, the second region having a surface located lower than that of the first region, and the second region being connected to the first region.

Furthermore, Rhee does not teach or suggest "a post oxide film formed on the second region, containing silicon and oxygen and arranged to be in contact with the gate electrode and the gate insulating film," as recited, *inter alia*, in Applicants' claim 1. According to Rhee's Figure 7, there is no post oxide film either covering (along channel length cross-sectional view, if it were shown) or deposited next to (along the channel width cross-sectional view, as shown) poly-Si gate electrodes 62 and 64. In contrast, Rhee's oxide film 80 is a field oxide film, which is completely different from Applicants' claimed post oxide film.

Teramoto fails to cure the deficiencies of Rhee, since Teramoto also does not teach or suggest the recitations of Applicants' present invention which are not taught or suggested in Rhee. Furthermore, even though Teramoto does not disclose or suggest all the features of Applicants' claimed invention, the inclusion of Teramoto does not render the recitations of Applicants' independent or dependent claims obvious when combined with Rhee. Merely because Teramoto discloses a "thin gate insulating film 506 of SiO_xN_y" (Teramoto's Figure 10C and column 18, line 37), does not mean that one would find it obvious to then use Teramoto's film in combination with Rhee to result in Applicants' claimed invention.

The Examiner does not show that there is a suggestion or motivation to modify Rhee with Teramoto to result in Applicants' claimed invention, and does not show that there is a reasonable expectation of success from doing so. There is no suggestion or reasonable expectation of success in Rhee to modify its disclosure in a manner that results in Applicants' claimed invention. It is clear, as shown above, that Rhee does not teach "a semiconductor substrate

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having a main plane in which a channel of a transistor is formed, the semiconductor substrate comprising a first region and a second region defined in a section taken along a direction of a channel length, the second region having a surface located lower than that of the first region, and the second region being connected to the first region," or "a post oxide film formed on the second region, containing silicon and oxygen and arranged to be in contact with the gate electrode and the gate insulating film," as recited in Applicants' claimed invention. As a matter of course, since neither structure taught by Rhee or Teramoto results in Applicants' claimed invention, it could not be obvious to combine Rhee with Teramoto in order to achieve the present claimed invention. Even if Teramoto were to be combined with Rhee to result in the present invention, which it cannot, Applicants respectfully point out to the Examiner that it "is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art" (see *In re Wesslau*, 147 U.S.P.Q. 391, C.C.P.A. 1965). See also M.P.E.P. § 2141.02, 8th Ed., Aug. 2001. Furthermore, since Teramoto does not cure the deficiencies of Rhee to result in Applicants' present invention, Teramoto does not provide motivation to modify Rhee or show that there would be an expectation of success from doing so.

Therefore, Applicants submit that claim 1 is patentable over Rhee in view of Teramoto, as are claims 2 – 4, at least by virtue of their dependence from allowable base claim 1. Therefore, Applicants respectfully submit that the Examiner should withdraw the 35 U.S.C. § 103(a) rejection.

Regarding the 35 U.S.C. § 103(a) rejection of claims 5 and 6 under 35 U.S.C. § 103(a) as unpatentable over Rhee and Teramoto as applied to claim 1 and further in view of Takemura;

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and the rejection of claim 7 under 35 U.S.C. § 103(a) as unpatentable over Rhee, Teramoto, and Takemura as applied to claim 5 and further in view of Tomita; the Examiner introduced Takemura for presumably teaching "a field effect device with a phosphorous (n-type) doped polysilicon gate," and Tomita for presumably teaching "a tunnel oxide film" (Office Action, page 6). Takemura and Tomita do not cure the deficiencies of Rhee and Teramoto to teach or suggest each and every recitation of Applicants' base claim 1, as already argued above pertaining to Rhee and Teramoto. Takemura's Figure 5A – 5F, for example, only depicts a cross section view of a crystallized Si thin film transistor (TFT) (column 7, line 30) taken along the channel width (between source/drain 27 and 28 in Figure 5C), and does not teach or suggest at least Applicants' claimed post oxide film. Likewise, Tomita's Figure 14C, for example, only depicts a cross section view of a semiconductor device (column 12, lines 40 – 65) taken along the channel width (between source/drain 17 in Figure 14C), and does not teach or suggest at least Applicants' claimed post oxide film. Therefore, neither Takemura nor Tomita, taken alone or in combination, can combine with Rhee and Teramoto to disclose or suggest each and every recitation of Applicants' claimed invention.

Since Applicants have already shown that Rhee and Teramoto, taken alone or in combination, cannot result in the present claimed invention, it is also clear that Rhee, Teramoto, and Takemura, or Rhee, Teramoto, Takemura, and Tomita, also taken alone or in combination, fail to meet all of the recitations of Applicants' claimed invention. Applicants submit that for at least the reasons argued above, claim 1 is already deemed patentable over Rhee in view of Teramoto, and therefore Applicants' claims 5 and 7 are patentable at least by virtue of their dependence from allowable base claim 1. (The rejection of claim 6 has been rendered moot by the cancellation of this claim.)

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Therefore, Applicants submit that claims 5 and 7 are patentable over Rhee, Teramoto, and Takemura, and Rhee, Teramoto, Takemura, and Tomita, respectively, for at least the reasons argued above, and by virtue of their dependence from allowable base claim 1. Therefore, Applicants respectfully submit that the Examiner should withdraw the 35 U.S.C. § 103(a) rejections of claims 5 – 7.

If, after consideration of the above arguments, the Examiner should continue to dispute the patentability of the claims, Applicants hereby "seasonably traverse" the Examiner's "official notice" statements on pages 3 and 7 of the Office Action and request that the Examiner cite a competent-reference in support of his or her position or supply an appropriate fact-based affidavit, or else withdraw the rejection." See M.P.E.P. § 2144.03, p.2100-129, 8th Ed. Applicants point out to the Examiner that other materials, such as silicon oxides, silicon nitrides, silicon oxynitrides, or even aerogels, all have "excellent dielectric strength properties" (Office Action, page 3); and that choosing an individual material for inclusion in a given invention is not just a matter of mere design choice. Merely taking "official notice that the use of silicon dioxide for field oxide components in the art of semiconductor devices has been well known … for a long time" (Office Action, page 3), and "official notice that the same obviousness considerations … apply to a floating gate electrode as to any other gate electrode" (Office Action, page 7), does not establish the obviousness of choosing a particular material in the device of the present invention.

At least for the abovementioned reasons, Applicants respectfully submit that independent claim 1 should be allowed, as should claims 2 – 5 and 7, at least by virtue of their dependence from allowable base claim 1.

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In view of the foregoing, Applicants respectfully request that the Examiner withdraw the rejection of claims 1 – 7 under 35 U.S.C. § 103(a), as detailed at the beginning of this Amendment. A favorable action is requested.

If any extension of time is required under 37 C.F.R. § 1.136 to obtain entry of this response, and not requested by attachment, such extension is hereby requested. If there are any fees due under 37 C.F.R. § 1.16 or 1.17 that are not enclosed, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge those fees to our Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: January 10, 2002

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APPENDIX TO AMENDMENT OF January 10, 2002

Version of Claims with Markings to Show Changes Made

AMENDMENTS TO THE CLAIMS:

Please amend claims 1 – 5 and 7 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a main plane in which a channel of a transistor is formed, [which has] the semiconductor substrate comprising a first region and a second region defined in a section taken along a direction of a channel length, the second region having a surface located lower than that of the first region, and the second region being connected to the first region [having the surface which is lower than the surface of the first region such that the first region and the second region are connected to each other];

a [first] gate insulating film formed on the first region and containing silicon, nitrogen and oxygen;

a [conductive film] gate electrode formed on the [first] gate insulating film and containing silicon; and

a [second insulating] post oxide film formed on the second region, containing silicon and oxygen and arranged to be in contact with the [conductive film] gate electrode and the [first] gate insulating film.

2. (Amended) A semiconductor device according to claim 1, wherein a portion of the [first] gate insulating film which is in contact with the semiconductor substrate contains nitrogen at a concentration higher than the concentration in a residual portion of the [first] gate insulating film.

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3. (Amended) A semiconductor device according to claim 2, wherein the concentration of nitrogen in a portion of the [first] gate insulating film which is in contact with the semiconductor substrate is 5×10^{13} cm^{-2} or higher.

4. (Amended) A semiconductor device according to claim 1, wherein the [second insulating] post oxide film further contains nitrogen, and a portion of the [second insulating] post oxide film which is in contact with the semiconductor substrate and the [conductive] gate electrode film has a concentration higher than the concentration in the residual portion of the [second insulating] post oxide film.

5. (Amended) A semiconductor device according to claim 1, wherein the [first] gate insulating film is a silicon oxide film containing nitrogen, and the [conductive film] gate electrode is a polycrystalline silicon film containing a dopant.

7. (Amended) A semiconductor device according to claim 5, wherein the [first] gate insulating film is a tunnel gate insulating film, and the [conductive film] gate electrode is a floating gate electrode.

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